What is claimed is:

1. A circuit arrangement for use in communicating multiple signals over a common signal path between first and second clock domains during hardware-based logic emulation, wherein the first clock domain is emulated via a first multi-step evaluation cycle and the second domain is emulated via a second multi-step evaluation cycle, the circuit arrangement comprising:

(a) a buffer interposed in a common signal path between first and second clock domains, the buffer including first and second locations, the first location associated with a first evaluation step in the first multi-step evaluation cycle and a first evaluation step in the second multi-step evaluation cycle, and the second location associated with a second evaluation step in the first multi-step evaluation cycle and a second evaluation step in the second multi-step evaluation cycle; and

(b) logic circuitry coupled to the buffer, the logic circuitry configured to store in the first location of the buffer a first time-multiplexed signal output over the common signal path by the first clock domain during the first evaluation step in the first multi-step evaluation cycle, and to store in the second location of the buffer a second time-multiplexed signal output over the common signal path by the first clock domain during the second evaluation step in the first multi-step evaluation cycle, the logic circuit further configured to output the first time-multiplexed signal stored in the first location over the common signal path to the second clock domain during the first evaluation step in the second multi-step evaluation cycle, and to output the second time-multiplexed signal stored in the second location over the common signal path to the second clock domain during the second evaluation step in the second multi-step evaluation cycle.

2. The circuit arrangement of claim 1, wherein the buffer comprises a multi-port array including a write port and a read port, and wherein the logic circuitry comprises a write control circuit and a read control circuit respectively coupled to the write port and read port of the multi-port array, the write control circuit configured to

control storage of signals from the first clock domain in the multi-port array, and the read control circuit configured to control output of signals from the multi-port array to the second clock domain.

3. The circuit arrangement of claim 2, wherein each of the write and read control circuits includes a counter.

4. The circuit arrangement of claim 3, wherein the counter in the write control circuit is configured to be incremented during each evaluation step in the first multi-step evaluation cycle, and wherein the counter in the read control circuit is configured to be incremented during each evaluation step in the second multi-step evaluation cycle.

5. The circuit arrangement of claim 4, wherein the counter in the write control circuit is configured to be reset for each first multi-step evaluation cycle, and wherein the counter in the read control circuit is configured to be reset for each second multi-step evaluation cycle.

6. The circuit arrangement of claim 4, wherein the counter in the first multi-step evaluation cycle maintains a current evaluation step number for the first clock domain, wherein the counter in the second multi-step evaluation cycle maintains a current evaluation step number for the second clock domain, wherein the read and write control circuits are each configured to use the respective current evaluation step numbers stored in the respective counters to address the multi-port array.

7. The circuit arrangement of claim 1, wherein the first and second multi-step evaluation cycles have different numbers of evaluation steps from one another.

8. The circuit arrangement of claim 1, wherein the buffer is further interposed within a second common signal path between the first and second clock domains, and wherein the logic circuitry is further configured to store in the buffer time-multiplexed

signals output over the second common signal path by the first clock domain concurrently with storing time-multiplexed signals output over the first common signal path, and to output over the second common signal path from the buffer to the second clock domain, the time-multiplexed signals stored in the buffer.

9. The circuit arrangement of claim 1, wherein the first and second locations are each a plurality of bits wide, wherein the buffer is interposed within a multi-bit common signal path between the first and second clock domains, and wherein the logic circuitry is further configured to stored in the buffer multi-bit time-multiplexed signals output over the multi-bit common signal path by the first clock domain, and to output over the multi-bit common signal path from the buffer to the second clock domain, the multi-bit time-multiplexed signals stored in the buffer.

10. A logic board comprising the circuit arrangement of claim 9.

11. A logic emulator comprising the circuit arrangement of claim 9.

12. The logic emulator of claim 11, further comprising a plurality of emulation processor integrated circuit devices, at least one of the emulation processor integrated circuit devices configured to emulate the first clock domain, and at least one other of the emulation processor integrated circuit devices configured to emulate the second clock domain.

13. The logic emulator of claim 12, further comprising a plurality of logic boards, each including a subset of the plurality of emulation processors, and wherein the common signal path extends between emulation processors disposed on different logic boards.

14. A circuit arrangement for use in communicating multiple signals over a common signal path between first and second clock domains during hardware-based logic emulation, wherein the first clock domain is emulated using a first multi-step evaluation cycle and the second domain is emulated using a second multi-step evaluation cycle, the circuit arrangement comprising:

(a) a buffer interposed between the first and second clock domains within the common signal path, the buffer including a plurality of locations, each of which associated with an evaluation step from each of the first and second multi-step evaluation cycles;

(b) a write control circuit responsive to a first step signal associated with a current evaluation step in the first multi-step evaluation cycle, the write control circuit configured to store a signal output over the common signal path by the first clock domain in a location in the buffer that is associated with the current evaluation step in the first multi-step evaluation cycle; and

(c) a read control circuit responsive to a second step signal associated with a current evaluation step in the second multi-step evaluation cycle, the read control circuit configured to output a signal stored in a location in the buffer that is associated with the current evaluation step in the second multi-step evaluation cycle.

15. The circuit arrangement of claim 14, wherein the buffer comprises a multi-port array including a write port coupled to the write control circuit and a read port coupled to the read control circuit, wherein the write control circuit includes a counter configured to be incremented in response to the first step signal, and wherein the read control circuit includes a counter configured to be incremented in response to the second step signal.

16. The circuit arrangement of claim 15, wherein the counter in the write control circuit is configured to be reset for each first multi-step evaluation cycle, and wherein the counter in the read control circuit is configured to be reset for each second multi-step evaluation cycle.

17. The circuit arrangement of claim 15, wherein the counter in the first multi-step evaluation cycle maintains a current evaluation step number for the first clock domain, wherein the counter in the second multi-step evaluation cycle maintains a current evaluation step number for the second clock domain, wherein the read and write control circuits are each configured to use the respective current evaluation step numbers stored in the respective counters to address the multi-port array.

18. The circuit arrangement of claim 14, wherein the first and second multi-step evaluation cycles have different numbers of evaluation steps from one another.

19. A method of communicating multiple signals over a common signal path between first and second clock domains during hardware-based logic emulation, the method comprising:

(a) during each of a first plurality of evaluation steps in an evaluation cycle for the first clock domain, communicating a signal associated with such evaluation step across the common signal path from the first clock domain to a buffer that has a plurality of locations, and storing the communicated signal in a location among the plurality of locations in the buffer that is associated with such evaluation step; and

(b) during each of a second plurality of evaluation steps in an evaluation cycle for the second clock domain, wherein each of the second plurality of evaluation steps is associated with a location among the plurality of locations, communicating a signal from the location in the buffer that is associated with such evaluation step from the second plurality of evaluation steps to the second clock domain.

20. The method of claim 19, wherein communicating the signal associated with each evaluation step in the evaluation cycle for the first clock domain includes incrementing a first counter for each such evaluation step, and wherein communicating the signal from the location associated with each evaluation step in the evaluation cycle for the second clock domain includes incrementing a second counter for each such evaluation step.

21. The method of claim 20, further comprising resetting the first counter for each evaluation cycle for the first clock domain, and resetting the second counter for each evaluation cycle for the second clock domain.

22. A method of communicating multiple signals over a common signal path between first and second clock domains during hardware-based logic emulation, wherein the first clock domain is emulated via a first multi-step evaluation cycle that includes first and second evaluation steps and the second domain is emulated via a second multi-step evaluation cycle that includes first and second evaluation steps, the method comprising:

(a) during the first evaluation step in the first multi-step evaluation cycle, receiving a first time-multiplexed signal output over the common signal path by the first clock domain and storing the first time-multiplexed signal in a first location in a buffer interposed in the common signal path, wherein the first location is associated with the first evaluation step in the first multi-step evaluation cycle and the first evaluation step in the second multi-step evaluation cycle;

(b) during the second evaluation step in the first multi-step evaluation cycle, receiving a second time-multiplexed signal output over the common signal path by the first clock domain and storing the second time-multiplexed signal in a second location in the buffer, wherein the second location is associated with the second evaluation step in the first multi-step evaluation cycle and the second evaluation step in the second multi-step evaluation cycle;

(c) during the first evaluation step in the second multi-step evaluation cycle, communicating the first time-multiplexed signal stored in the first location over the common signal path to the second clock domain; and

(d) during the second evaluation step in the second multi-step evaluation cycle, communicating the second time-multiplexed signal stored in the second location over the common signal path to the second clock domain.

23. The method of claim 22, wherein the buffer comprises a multi-port array including a write port and a read port, the method further comprising incrementing a first counter for each evaluation step in the first multi-step evaluation cycle, incrementing a second counter for each evaluation step in the second multi-step

evaluation cycle, and utilizing the first and second counters to respectively address the write and read ports of the multi-port array.

24. The method of claim 20, further comprising resetting the first counter for each first multi-step evaluation cycle, and resetting the second counter for each second multi-step evaluation cycle.